AMENDMENTS TO THE CLAIMS

Kindly amend the claims as follows:

1. (currently amended) A circuit, comprising:

a control circuit adapted to generate at least a first and second signal in response to a test enable signal;

a differential driver circuit coupled to said control circuit, having a differential input node and a differential output node and adapted to receive a differential input signal at said differential input node, amplify said differential input signal and transmit a differential output signal onto said differential output node in response said first signal, said differential driver circuit further comprising:

a plurality of FIR latches coupled to said differential input node and adapted to store said differential input signal;

a plurality of preamplifier circuits coupled to said FIR latches and adapted to amplify said differential input signal, wherein said preamplifier circuits are enabled in response to said first signal;

a driver output stage coupled to said preamplifier circuits and adapted to transmit said differential output signal; and

a current DAC circuit coupled to said driver output stage and adapted to set drive strength of said driver output stage in response to a plurality of IDAC control signals;

a programmable termination impedance circuit coupled to said control circuit and said differential output node, adapted to generate a differential termination impedance at said differential output node in response to said second signal; and

a differential receiver circuit coupled to said control circuit and said differential output node, adapted to receive said differential output signal, convert

said differential output signal to a single ended signal and transmit said single ended signal in response to said test enable signal.

2. (original) The circuit of claim 1 further comprising:

a first shift-register-latch circuit coupled to said differential input node and adapted to store said differential input signal; and

a second shift-register-latch circuit coupled to said differential receiver circuit and adapted to store said transmitted single ended signal.

3. Canceled.

4. (currently amended) The circuit of ~~claim 3~~ claim 1, wherein only one of said preamplifier circuits is enabled during a test sequence.

5. (currently amended) The circuit of ~~claim 3~~ claim 1, further comprising a third shift-register-latch circuit coupled to said current DAC circuit and adapted to store said IDAC control signals.

6 - 7. Canceled.

8. (currently amended) The circuit of ~~claim 7~~claim 21, wherein said differential termination impedance is skewed at said first node and said second node when said test enable signal is active and said differential termination impedance is matched at said first node and said second node when said test enable signal is deactive.

9. (currently amended) The circuit of ~~claim 7~~ claim 21, wherein a first six of said resistor components are coupled to said first node and a second six of said resistor components are coupled to said second node.

10. (original) The circuit of claim 9, wherein a first resistor of said first six resistor components is approximately 53 Ohms, a second resistor of said first six resistor components is approximately 71 Ohms, a third resistor of said first six resistor components is approximately 144 Ohms, a fourth resistor of said first six resistor components is approximately 287 Ohms, a fifth resistor of said first six resistor components is approximately 554 Ohms, a sixth resistor of said first six resistor components is approximately 3001 Ohms, a first resistor of said second six resistor components is approximately 53 Ohms, a second resistor of said second six resistor components is approximately 71 Ohms, a third resistor of said second six resistor components is approximately 144 Ohms, a fourth resistor of said second six resistor components is approximately 287 Ohms, a fifth resistor of said second six resistor components is approximately 554 Ohms, and a sixth resistor of said second six resistor components is approximately 3001 Ohms.

11. Canceled.

12. (currently amended) The circuit of ~~claim 11~~claim 22, wherein said differential receiver further comprises a second built-in offset voltage comparator circuit electrically coupled in parallel with said first built-in offset voltage comparator circuit and adapted to output a signal in response to said differential output signal and a second offset voltage, wherein said first built-in offset voltage comparator circuit and said second built-in offset voltage comparator circuit form a hysteresis comparator.

13. (original) The circuit of claim 12 wherein said hysteresis comparator is disabled when said second built-in offset voltage comparator circuit is disabled.

14. (currently amended) The circuit of ~~claim 11~~ claim 22, wherein said differential receiver circuit is disabled when said differential amplifier circuit is disabled.

15. (currently amended) The circuit of ~~claim 11~~ claim 22, wherein said output signal of said built-in offset voltage comparator is high when said received differential output signal is greater than said offset voltage and low otherwise.

16 - 20. Canceled.

Kindly add the following new claims:

21. (new) A circuit, comprising:

a control circuit adapted to generate at least a first and second signal in response to a test enable signal;

a differential driver circuit coupled to said control circuit, having a differential input node and a differential output node and adapted to receive a differential input signal at said differential input node, amplify said differential input signal and transmit a differential output signal onto said differential output node in response said first signal;

a programmable termination impedance circuit coupled to said control circuit and said differential output node, adapted to generate a differential termination impedance at said differential output node in response to said second signal, said programmable termination impedance circuit comprises a plurality of resistor components, each resistor component having an associated switch for selectively connecting that resistor component from a voltage source to said differential output node, wherein at least one, but less than all of said resistor components are coupled to a first node of said differential output node and a remainder of said resistor components are coupled to a second node of said differential output node; and

a differential receiver circuit coupled to said control circuit and said differential output node, adapted to receive said differential output signal, convert said differential output signal to a single ended signal and transmit said single ended signal in response to said test enable signal.

22. (new) A circuit, comprising:

a control circuit adapted to generate at least a first and second signal in response to a test enable signal;

a differential driver circuit coupled to said control circuit, having a differential input node and a differential output node and adapted to receive a differential input signal at said differential input node, amplify said differential input signal and transmit a differential output signal onto said differential output node in response said first signal;

a programmable termination impedance circuit coupled to said control circuit and said differential output node, adapted to generate a differential termination impedance at said differential output node in response to said second signal; and

a differential receiver circuit coupled to said control circuit and said differential output node, adapted to receive said differential output signal, convert said differential output signal to a single ended signal and transmit said single ended signal in response to said test enable signal, said differential receiver circuit comprising:

a differential amplifier circuit coupled to said differential output node and adapted to receive said differential output signal;

a built-in offset voltage comparator circuit coupled to said differential amplifier circuit and adapted to output a signal in response to said differential output signal and an offset voltage;

an output stage coupled to said differential amplifier circuit and said built-in offset voltage comparator circuit and adapted to transmit said single ended signal in response to said output signal of said built-in offset voltage comparator circuit; and

a level shifter circuit coupled to said output stage and adapted to transition power supply domains from an analog power supply domain to a digital power supply domain.

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